

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. <b>2885/85</b>	Serial No. <b>10/791,501</b>
	Applicant(s) <b>Vorbach et al.</b>	
	Filing Date <b>March 1, 2004</b>	Group Art Unit <b>2116</b>

## U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	RE37,195	May 29, 2001	Kean			
	4,667,190	May 1987	Fant et al.			
	4,972,314	November 1990	Getzinger et al.			
	5,010,401	April 1991	Murakami et al.			
	5,034,914	July 1991	Osterlund			
	5,041,924	August 1991	Blackborow et al.			
	5,099,447	March 1992	Myszewski			
	5,193,202	March 9, 1993	Jackson et al.			
	5,237,686	August 1993	Asano et al.			
	5,327,125	July 1994	Iwase et al.			
	5,418,953	May 1995	Hunt et al.			
	5,343,406	Aug 30, 1994	Freeman et al.			
	5,537,580	July 1996	Giomi et al.			
	5,550,782	Aug 27, 1996	Cliff et al.			
	5,625,836	Apr 29, 1997	Barker et al.			
	5,646,544	Jul 8, 1997	Iadanza			
	5,646,545	Jul 8, 1997	Trimberger et al.			
	5,737,565	April 1998	Mayfield			
	5,754,459	May 19, 1998	Telikepalli			
	5,781,756	Jul 14, 1998	Hung			
	5,801,547	Sep 1, 1998	Kean			
	5,831,448	Nov 3, 1998	Kean			
	5,857,097	January 1999	Henzinger et al.			
	5,870,620	Feb 9, 1999	Kadosumi et al.			
	5,889,533	Mar 30, 1999	Lee			
	5,978,583	November 1999	Ekanadham et al.			
	5,933,023	Aug 3, 1999	Young			
	5,996,143	Oct 12, 1999	Breternitz, Jr.			
	6,044,030	Mar 28, 2000	Zhang et al.			
	6,084,429	July 2000	Trimberger			
	6,105,106	August 2000	Manning			
	6,137,307	October 2000	Iwanczuk et al.			
	6,154,048	November 2000	Iwanczuk et al.			
	6,154,049	Nov 28, 2000	New			
	6,157,214	December 5, 2000	Marshall			
	6,201,406	March 2001	Iwanczuk et al.			
	6,204,687	March 2001	Schultz et al.			
	6,215,326	April 10, 2001	Jefferson et al.			

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No. 2885/85	Serial No. 10/791,501
Applicant(s) Vorbach et al.	
Filing Date March 1, 2004	Group Art Unit 2116

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,252,792	June 26, 2001	Marshall et al.			
	6,262,908	July 17, 2001	Marshall et al.			
	6,311,265	October 2001	Beckerle et al.			
	6,373,779	Apr 16, 2002	Pang et al.			
	6,353,841	March 5, 2002	Marshall et al.			
	6,362,650	Mar 26, 2002	New et al.			
	6,427,156	Jul 30, 2002	Chapman et al.			
	6,430,309	August 2002	Pressman et al.			
	6,434,642	Aug 13, 2002	Camilleri et al.			
	6,438,747	August 2002	Schreiber et al.			
	6,487,709	November 2002	Keller et al.			
	6,523,107	February 18, 2003	Stansfield et al.			
	6,542,394	April 1, 2003	Marshall et al.			
	6,553,395	April 22, 2003	Marshall et al.			
	6,567,834	May 20, 2003	Marshall et al.			
	6,631,487	October 2003	Abramovici et al.			
	6,658,564	December 2003	Smith et al.			
	6,754,805	June 2004	Yujen Juan			
	6,820,188	November 16, 2004	Stansfield et al.			
	6,847,370	January 2005	Baldwin et al.			
	6,874,108	March 2005	Abramovici et al.			
	6,977,649	December 2005	Baldwin et al.			
	7,000,161	February 2006	Allen et al.			
	7,007,096	February 2006	Lisitsa et al.			
	7,038,952	May 2, 2006	Zack et al.			
	7,210,129	April 2007	May et al.			
	7,340,596	March 2008	Croslan et al.			
	7,350,178	March 2008	Croslan et al.			
	2001/001860	May 2001	Bieu			
	2003/062922	Apr 3, 2003	Douglass et al.			
	2003/061542	March 2003	Bates et al.			
	2005/0144210	Jun 30, 2005	Simkins et al.			
	2005/0144212	Jun 30, 2005	Simkins et al.			
	2005/0144215	Jun 30, 2005	Simkins et al.			
	2005/066213	March 2005	Vorbach et al.			

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. <b>2885/85</b>	Serial No. <b>10/791,501</b>
	Applicant(s) <b>Vorbach et al.</b>	
	Filing Date <b>March 1, 2004</b>	Group Art Unit <b>2116</b>

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	2006/0230094	Oct 12, 2006	Simkins et al.			
	2006/0130096	Oct 12, 2006	Thendean et al.			

**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	196 54 593	July 2, 1998	Germany			Abstract	
	EP I 669 885	Jun 14, 2006	EPO			Abstract	
	WO98/10517	March 12, 1998	PCT				
	WO00/49496	August 24, 2000	PCT				
	WO02/50665	June 27, 2002	PCT				
	WO 2004/053718	June 24, 2004	PCT				
	WO05/045692	March 19, 2005	PCT				
	05-509184	December 16, 2003	Japan			English Equivalent = USP 5,193,202 cited above	
	08069447	March 12, 1996	Japan			Abstract	
	2001-500682	January 16, 2001	Japan			Abstract	
	2000-201066	July 18, 2000	Japan			Abstract	

**OTHER DOCUMENTS**

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Altera, "Flex 8000 Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-62.
	Altera, "Flex 10K Embedded Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-128.
	Atmel, 5-K-50K Gates Coprocessor FPGA with Free Ram, Data Sheet, July 2006, 55 pages.
	Atmel, FPGA-based FIR Filter Application Note, September 1999, 10 pages.
	Atmel, "An Introduction to DSP Applications using the AT40K FPGA," FPGA Application Engineering, San Jose, CA, April 2004, 15 pages.
	Atmel, Configurable Logic Design & Application Book, Atmel Corporation, 1995, pp. 2-19 through 2-25.
	Atmel, Field Programmable Gate Array Configuration Guide, AT6000 Series Configuration Data Sheet, September 1999, pp. 1-20.
	Bacon, D. et al., "Compiler Transformations for High-Performance Computing," ACM Computing Surveys, 26(4):325-420 (1994).

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No.  
2885/85Serial No.  
10/791,501Applicant(s)  
Vorbach et al.Filing Date  
March 1, 2004Group Art Unit  
2116

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Becker, J. et al., "Architecture, Memory and Interface Technology Integration of an Industrial/Academic Configurable System-on-Chip (CSoC)," IEEE Computer Society Annual Workshop on VLSI (WVLSI 2003), (February 2003), 6 pages.
	Becker, J., "Configurable Systems-on-Chip (CSoC)," (Invited Tutorial), Proc. of 9th Proc. of XV Brazilian Symposium on Integrated Circuit, Design (SBCCI 2002), (September 2002), 6 pages.
	Cardoso, J.M.P. et al., "A novel algorithm combining temporal partitioning and sharing of functional units," University of Algarve, Faro, Portugal, 2001 IEEE, pp. 1-10.
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0702, 2007, pp. 1-15, <a href="http://www.clearspeed.com">www.clearspeed.com</a> .
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0306, 2006, pp. 1-14, <a href="http://www.clearspeed.com">www.clearspeed.com</a> .
	Cronquist, D. et al., 'Architecture Design of Reconfigurable Pipelined Datapaths,' Department of Computer Science and Engineering, University of Washington, Seattle, WA, Proceedings of the 20 <sup>th</sup> Anniversary Conference on Advanced Research in VSLI, 1999, pp. 1-15.
	DeHon, Andre, "Reconfigurable Architectures for General-Purpose Computing," Massachusetts Institute of Technology, Technical Report AITR-1586, October 1996 (1996-10), XP002445054, Cambridge, MA, pp. 1-353.
	Diniz, P., et al., "A behavioral synthesis estimation interface for configurable computing," University of Southern California, Marina Del Rey, CA, 2001 IEEE, pp. 1-2.
	Ebeling, C. et al., "Mapping Applications to the RaPiD Configurable Architecture," Department of Computer Science and Engineering, University of Washington, Seattle, WA, <u>FPGAs for Custom Computing Machines, 1997. Proceedings. The 5th Annual IEEE Symposium</u> , Publication Date: 16-18 Apr 1997, 10 pages.
	Equator, Pixels to Packets, Enabling Multi-Format High Definition Video, Equator Technologies BSP-15 Product Brief, <a href="http://www.equator.com">www.equator.com</a> , 2001, 4 pages.
	Freescale Slide Presentation, An Introduction to Motorola's RCF (Reconfigurable Compute Fabric) Technology, Presented by Frank David, Launched by Freescale Semiconductor, Inc., 2004, 39 pages.
	Genius, D. et al., "A Case for Array Merging in Memory Hierarchies," Proceedings of the 9th International Workshop on Compilers for Parallel Computers, CPC'01 (June 2001), pp. 1-10.
	Hartenstein, R. et al., "A new FPGA architecture for word-oriented datapaths," Proc. FPL'94, Springer LNCS, September 1994, pp. 144-155.
	Hwang, K., "Computer Architecture and Parallel Processing," Data Flow Computers and VLSI Computations, XP-002418655, 1985 McGraw-Hill, Chapter 10, pp. 732-807.
	Inside DSP, "Ambric Discloses Massively Parallel Architecture," August 23, 2006, <a href="http://insidedsp.com/tabid/64/articleType/ArticleView/articleId/155/Defa...">HTTP://insidedsp.com/tabid/64/articleType/ArticleView/articleId/155/Defa...</a> , 2 pages.
	Intel, Intel MXP5800/MXP5400 Digital Media Processors, Architecture Overview, June 2004, Revision 2.4, pp. 1-14.
	Kaul, M., et al., "An automated temporal partitioning and loop fission approach of FPGA based reconfigurable synthesis of DSP applications," University of Cincinnati, Cincinnati, OH, ACM 1999, pp. 616-622.
	Kean, T.A., "Configurable Logic: A Dynamically Programmable Cellular Architecture and its VLSI Implementation," University of Edinburgh (Dissertation) 1988, pp. 1-286
	Kean, T., et al., "A Fast Constant Coefficient Multiplier for the XC6200," Xilinx, Inc., Lecture Notes in Computer Science, Vol. 1142, Proceedings of the 6 <sup>th</sup> International Workshop of Field-Programmable Logic, 1996, 7 pages.
	Kim et al., "A Reconfigurable Multifunction Computing Cache Architecture," IEEE Transactions on Very Large Scale Integration (VLSI) Systems Volume 9, Issue 4, Aug 2001 Page(s):509 - 523.
	Larsen, S. et al., "Increasing and Detecting Memory Address Congruence," Proceedings of the 2002 IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT'02), pp. 18-29 (September 2002).

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. <b>2885/85</b>	Serial No. <b>10/791,501</b>
Applicant(s) <b>Vorbach et al.</b>		
Filing Date <b>March 1, 2004</b>	Group Art Unit <b>2116</b>	

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Maxfield, C., "Logic that mutates while-u-wait," EDN Access 1996, EDN Magazine, <a href="http://www.edn.com/index">www.edn.com/index</a> , 4 pages.
	Mei, Bingfeng, "A Coarse-Grained Reconfigurable Architecture Template and Its Compilation Techniques," Katholieke Universiteit Leuven, PhD Thesis, January 2005, IMEC vzw, Universitair Micro-Electronica Centrum, Belgium, pp. 1-195 (and Table of Contents).
	Mei, Bingfeng, et al., "Design and Optimization of Dynamically Reconfigurable Embedded Systems," IMEC vzw, 2003, Belgium, 7 pages, <a href="http://www.imec.be/reconfigurable/pdf/ICERSA_01_design.pdf">http://www.imec.be/reconfigurable/pdf/ICERSA_01_design.pdf</a>
	Miyamori, T. et al., "REMARCS: Reconfigurable Multimedia Array Coprocessor," Computer Systems Laboratory, Stanford University, IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS E SERIES D, 1999; (abstract): Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays, p.261, February 22-25, 1998, Monterey, California, United States, pp. 1-12.
	Muchnick, S., "Advanced Compiler Design and Implementation" (Morgan Kaufmann 1997), Table of Contents, 11 pages.
	Murphy, C., "Virtual Hardware Using Dynamic Reconfigurable Field Programmable Gate Arrays," Engineering Development Centre, Liverpool John Moores University, UK, GERI Annual Research Symposium 2005, 8 pages.
	Nageldinger, U., "Design-Space Exploration for Coarse Grained Reconfigurable Architectures," (Dissertation) Universitaet Kaiserslautern, 2000, Chapter 2, pp. 19-45.
	Olukotun, K., "The Case for a Single-Chip Microprocessor," ACM Sigplan Notices, ACM, Association for Computing Machinery, New York, Vol. 31, No. 9, September 1996 (1996-09-00) pp. 2-11.
	PACT Corporation, "The XPP Communication System," Technical Report 15 (2000), pp. 1-16.
	Saleeba, Z.M.G., "A Self-Reconfiguring Computer System," Department of Computer Science, Monash University (Dissertation) 1998, pp. 1-306.
	Schmidt, H. et al., "Behavioral synthesis for FGPA-based computing," Carnegie Mellon University, Pittsburgh, PA, 1994 IEEE, pp. 125-132.
	Singh, H. et al., "MorphoSys: An Integrated Reconfigurable System for Data-Parallel Computation-Intensive Applications," University of California, Irvine, CA. and Federal University of Rio de Janeiro, Brazil, 2000, IEEE Transactions on Computers, pp. 1-35.
	Soni, M., "VLSI Implementation of a Wormhole Run-time Reconfigurable Processor," June 2001, (Masters Thesis)Virginia Polytechnic Institute and State University, 88 pages.
	Vasell et al., "The Function Processor: A Data-Driven Processor Array for Irregular Computations," Chalmers University of Technology, Sweden, pp. 1-21.
	Waingold, E., et al., "Baring it all to software: Raw machines," IEEE Computer, September 1997, at 86-93.
	Weinhardt, Markus et al., "Memory Access Optimization for Reconfigurable Systems," IEEE Proceedings Computers and Digital Techniques, 48(3) (May 2001).
	Wolfe, M. et al., "High Performance Compilers for Parallel Computing" (Addison-Wesley 1996), Table of Contents, 11 pages.
	XILINX, "XC6200 Field Programmable Gate Arrays," April 24, 1997, Xilinx product description, pp. 1-73.
	XILINX, "XC3000 Series Field Programmable Gate Arrays," November 6, 1998, Xilinx product description, pp. 1-76.
	XILINX, "XC4000E and XC4000X Series Field Programmable Gate Arrays," May 14, 1999, Xilinx product description, pp. 1-68.
	XILINX, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays," July 17, 2002, Xilinx Production Product Specification, pp. 1-118
	XILINX, "Virtex-II and Virtex-II Pro X FPGA User Guide," March 28, 2007, Xilinx user guide, pp. 1-559.
	Zhang et al., "Abstract: Low-Power Heterogeneous Reconfigurable Digital Signal Processors with Energy-Efficient Interconnect Network," U.C. Berkeley (2004), pp. 1-120.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. <b>2885/85</b>	Serial No. <b>10/791,501</b>
	Applicant(s) <b>Vorbach et al.</b>	
	Filing Date <b>March 1, 2004</b>	Group Art Unit <b>2116</b>

<b>EXAMINER'S INITIALS</b>	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.	
	Zima, H. et al., "Supercompilers for parallel and vector computers" (Addison-Wesley 1991), Table of Contents, 5 pages.	
<b>EXAMINER</b>	<b>DATE CONSIDERED</b>	
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		